Claims

What is claimed is:

1. A clock generator for generating a non-phase-modulated target clock signal based on a phase-modulated input signal, the clock generator comprising:

an arithmetic/logic circuit for calculating a period count value by counting a period of the input signal according to a reference clock having a predetermined frequency, calculating an average value by averaging a plurality of the period count values, and comparing the average value with the period count value for outputting a first control signal; and

a phase-locked loop connected to the arithmetic/logic circuit for generating the target signal according to the first control signal and the input signal, feeding the target signal back to the input of the phase-locked loop, and determining whether the target clock signal is to be synchronized with the input signal based on the logic level of the first control signal;

wherein when the first control signal corresponds to a first logic level, the phase-locked loop compares the target clock signal with the input signal to drive the target clock signal to be synchronized with the input signal, and when the first control signal corresponds to a second logic level, the phase-locked loop holds the target clock signal without driving the target clock signal to be synchronized with the input signal.

2. The clock generator of claim 1, wherein the arithmetic/logic circuit comprises:

a reference clock generator for generating the reference clock having a predetermined frequency;

a counter connected to the reference clock generator for calculating the period count value by counting a period of the input signal according to the reference clock;

a mean operation unit connected to the counter for calculating an average value by averaging a plurality of the period count values; and

a comparator connected to the counter and the mean operation unit for comparing the period count value with the average value.

3. The clock generator of claim 2, wherein the phase-locked loop comprises:

a phase-frequency detector connected to the comparator for generating a second control signal by comparing the target clock signal with the input signal, and for determining whether the second control signal is outputted according to the logic level of the first control signal;

a loop filter connected to the phase-frequency detector for generating a control voltage based on the second control signal; and

a voltage-controlled oscillator connected to the loop filter for controlling the frequency of the target clock signal based on the control voltage.

4. The clock generator of claim 3, wherein the phase-locked loop further comprises a second slicer connected to the phase-frequency detector and the voltage-controlled oscillator for slicing the target clock signal.

5. The clock generator of claim 3, wherein the loop filter comprises a charge pump circuit for controlling the control voltage based on the second control signal.

6. The clock generator of claim 1, wherein when the difference between the period count value and the average value is less than a critical value, the first control signal is set to a first logic level.

7. The clock generator of claim 1, wherein when the differences between a plurality of the consecutive period count values and the average value are all less than a critical value, the first control signal is set to a first logic level.

8. The clock generator of claim 1, wherein when the difference between the period count value and the average value is larger than a critical value, the first control signal is set to a second logic level.

9. The clock generator of claim 1, wherein when the differences between a plurality of the consecutive period count values and the average value are all larger than a critical value, the first control signal is set to a second logic level.

10. The clock generator of claim 1, wherein the clock generator further comprises:

a band-pass filter for extracting the input signal having a frequency within a predetermined band; and

a first slicer connected to the band-pass filter for slicing the input signal and forwarding the input signal to the arithmetic/logic circuit and the phase-locked loop.

11. The clock generator of claim 1 being applied to an optical drive, the optical drive is a DVD-R optical drive or a DVD-RW optical drive, the optical drive comprising an ADIP decoder for predicting a timing for the input of the first period corresponding to the next ADIP unit of the input signal and generating a second control signal to prohibit the phase-locked loop from driving the target clock signal to be synchronized with the input signal at a predetermined time before the timing of the input of the first period corresponding to the next ADIP unit of the input signal.

12. A clock generating method for generating a non-phase-modulated target clock signal based on a phased-modulated input signal,
the clock generating method comprising:
determining whether the target clock signal is to be synchronized with the input signal according to a first control signal for generating a second control signal;
generating a control voltage based on the second control signal; and
controlling the frequency of the target clock signal according to the control voltage;
wherein a period count value is generated by counting a period of the input signal according to a reference clock having a predetermined frequency and the logic level of the first control signal is determined by comparing the period count value with an average value.

13. The clock generating method of claim 12, wherein the generating method of the first control signal comprises:
generating a reference clock having a predetermined frequency;

calculating a period count value by counting a period of the input signal according to the reference clock; and generating the first control signal by comparing the period count value with an average value;

wherein the average value is an average of a plurality of the period count values.

14. The clock generating method of claim 13 further comprising:

initiating the average value with an initial value; and

calculating the average value by averaging a predetermined number of the period count values;

wherein when the average value equals the initial value, the method further comprises stopping comparing the average value with the period count value.

15. The clock generating method of claim 12, wherein when the first control signal equals to a first logic level, the method further comprises comparing the target clock signal with the input signal for driving the target clock signal to be synchronized with the input signal, and when the first control signal equals to a second logic level, the method further comprises holding the target clock signal without driving the target clock signal to be synchronized with the input signal.

16. The clock generating method of claim 15, wherein the first control signal corresponds to the second logic level when the difference between the period count value and the average value is larger than a critical value.

17. The clock generating method of claim 15, wherein the first control signal corresponds to the second logic level when

the differences between a plurality of the consecutive period count values and the average value are all larger than a critical value.

18. The clock generating method of claim 15, wherein the first control signal corresponds to the first logic level when the difference between the period count value and the average value is less than a critical value.

19. The clock generating method of claim 15, wherein the first control signal corresponds to the first logic level when the differences between a plurality of the consecutive period count values and the average value are all less than a critical value.

20. The clock generating method of claim 12 being applied to an optical drive, the optical drive is a DVD-R optical drive or a DVD-RW optical drive, the clock generating method further comprising predicting a timing for the input of the first period of the input signal and generating a second control signal for holding the target clock signal without driving the target clock signal to be synchronized with the input signal at a predetermined time before the timing of the input of the first period of the input signal.